



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,109	12/20/2001	Erik E. Erlandson	10016854-1	7028

7590 10/02/2006

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER

SONG, JASMINE

ART UNIT	PAPER NUMBER
----------	--------------

2188

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/032,109	<b>Applicant(s)</b> ERLANDSON ET AL.	
	<b>Examiner</b> Jasmine Song	<b>Art Unit</b> 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 18 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-14, 16-21, 23-28 and 31-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-14, 16-21 and 34-40 is/are allowed.
- 6) ☒ Claim(s) 23-28 and 31-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## Detailed Action

1. This office action is in response to RCE filed on 09/18/2006. Claims 15,22 and 29-30 are canceled, therefore, claims 1-14,16-21, 23-28 and 31-40 are pending in the application. All rejections and objections not explicitly repeated below are withdrawn.

## Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 23-28 and 31-33 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 23, the limitations "receiving an address strobe **with** a memory circuit; receiving a first address **with** the memory circuit...; generating a second address **with** the memory circuit.." are not clear or distinct. It is not clear as to how a column – address anticipation counter 14 receives an address strobe CAS with a memory circuit since the memory circuit is element 26 of the

Fig.5. (see Fig.5 and applicant's remarks filed on 09/18/2006, page 11, starting "for Example... a memory circuit 26). In claim 27, the limitations "receiving **with the memory circuit** during a data-transfer cycle a first address from a source external to **the memory circuit**" is not clear or distinct. It is not clear as to how a first address is received with the memory circuit to the memory circuit. In addition, it is not clear as to how to perform the step of receiving with the memory circuit since the memory circuit is element 26 of the Fig.5. (see Fig.5 and applicant's remarks filed on 09/18/2006, page 12-13, starting "for Example... a memory circuit 26). It is not possible from either the specification or the claim to determine the scope of this language or to determine the metes and bounds of the claims. For examination purposes, the claim 23 is interpreted as "receiving an address strobe **within** a memory circuit; receiving a first address **within** the memory circuit...; generating a second address **within** the memory circuit...; comparing the first address to the second address **within** the memory circuit". due to the ambiguities and confusion in claim 27 as cited above, the examiner will not speculate as to the intended meaning, therefore, the rejection has been maintained as shown below.

### **Claim Rejections - 35 USC § 102**

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2188

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Biggs et al., US 6,128,716.

Regarding claim 23, Biggs teaches that a method, comprising:

Receiving an address strobe within a memory circuit (Fig.1, a memory circuit is interpreted as the combination of memory controller 42 and DRAM 43);

receiving a first address within the memory circuit (it is taught as receiving INTERNAL ADDRESS has a value labeled R2C2, col.4, lines 57-59) during a data-transfer cycle (according to specification, a data-transfer cycle is a page mode cycle, see page 8, however, Biggs teaches page mode cycle such as page hit signal and Biggs mentioned terminating the page mode access);

generating a second address within the memory circuit (it is taught as generating another INTERNAL ADDRESS R3C3, col.4, lines 66-67) during the data-transfer cycle;

comparing the first address to the second address within the memory circuit (col.5, it is taught as comparing R3 and R2); and

terminating the data-transfer cycle (it is taught as terminating the page mode access by deactivating both RAS and CAS, col.5, lines 3-5) during which data is being transferred to or from a storage location residing at the second address (it is taught as data is being accessed to or from the R3C3 before terminating the page mode) if the first address does not have a predetermined relationship to the second address (it is taught as R3 is not equal to R2, it means a page miss mode).

Art Unit: 2188

Regarding claim 25, Biggs teaches that receiving a first address comprises receiving with a memory circuit a first address that is generated outside of the memory circuit (it is taught as input terminal for receiving address signals, col.3, lines 21-24); and generating a second address comprises generating a second address inside of the memory circuit (it is taught as an output terminal for providing M address signals, col.3, lines 21-24).

Regarding claims 24 and 26, Biggs teaches that terminating the cycle comprises terminating the cycle if the first address does not equal the second address (col.5, line 1-5); and enabling the cycle if the first address equals the second address (col.3, lines 60-65).

7. Claims 27-28 and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Ryan et al., US 5,966,724.

Regarding claim 27, Ryan teaches that a method, comprising:

generating a first address (it is taught as the generated internally address, col.5, lines 52) during a data-transfer cycle (according to specification, a data-transfer cycle is a page mode cycle, see page 8, however, Ryan teaches the burst access cycle and its implementation requires very little additional circuitry over the page mode DRAM);

comparing the first address to a predetermined value (col.5, lines 51-54, the predetermined value can be initial address in one embodiment or can be a predetermined number accesses in another embodiment);

Art Unit: 2188

terminating the data-transfer cycle (it is taught as terminating the burst access) during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value (it is taught as a match occurs, col.5, lines 54).

Regarding claim 28, Ryan teaches that further comprising enabling the cycle if the first address does not have the predetermined relationship to the predetermined value (col.5, lines 44-46).

Regarding claim 31, Ryan teaches further comprising disabling the cycle comprises disabling the cycle if the first address equals the predetermined value (col.5, lines 50-54); and enabling the cycle if the first address does not equal the predetermined value (col.5, lines 44-46).

Regarding claim 32, Ryan teaches that further comprising wherein generating a first address comprises generating the first address inside of a memory circuit (col.3, lines 5-8, it is considered the whole Fig.1 as a memory circuit); and

receiving with the memory circuit a second address from outside of the memory circuit (Fig.1, memory array 12 is considered as a memory circuit).

Regarding claim 33, Ryan teaches that further comprising loading the predetermined value into a memory that includes the storage location (it is taught as initial address has been latched or the burst counter counts the number of accesses).

### **Allowable Subject Matter**

8. Claims 1-14,16-21,34-40 are allowed.
9. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).
10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone



Art Unit: 2188

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Jasmine Song

Patent Examiner

September 26, 2006